WHAT IS CLAIMED IS:

1. A method of generating a multiple of a unit U, N times U, by a digital circuit, where U is a rational number and N is a natural number, comprising the steps of:

storing values A, B and C, where A, B and C are natural numbers, $A > 1$, $B > C$ and $U = A + C/B$;

generating a multiple of A, N times A, and a multiple of C, N times C;

comparing the value B with the multiple of C;

modifying the multiple of A according to the result of the comparing step; and

outputting the modified multiple of A as the multiple of U.

2. The method claimed in claim 1, wherein when the result of the comparing step is that the multiple of C is equal to or larger than the value B, the modifying step comprising the steps of:

modifying the multiple of A; and

subtracting the value B from the multiple of C.

3. The method claimed in claim 1, wherein when the result of the comparing step is that the multiple of C is equal to or larger than a value MB, where M is a predetermined natural number, the modifying step comprising the steps of:

modifying the multiple of A; and

subtracting the value MB from the multiple of C.

4. The method claimed in claim 1, wherein the C/B represents a repeating decimal.

5. A method of generating a dependent variable of a periodic function whose independent variable is a multiple of a unit U, N times U, by a digital circuit, where U is a rational number and N is a natural number, comprising the steps of:

storing values A, B and C, where A, B and C are natural numbers, $A > 1$, $B > C$ and $U = A + C/B$;

generating a multiple of A, N times A, and a multiple of C, N times C;

comparing the value B with the multiple of C;

modifying the multiple of A according to the result of the comparing step; and

extracting a value corresponding to the modified multiple of A from a function table, which represents relationship between the dependent and independent variables of the periodic function and is previously stored in a memory device, as the dependent variable corresponding to the multiple of U.

6. The method claimed in claim 5, wherein when the result of the comparing step is that the multiple of C is equal to or larger than the value B, the modifying step comprising the steps of:

modifying the multiple of A; and

subtracting the value B from the multiple of C.

7. The method claimed in claim 5, wherein when the result of the comparing step is that the multiple of C is equal to or larger than a value MB, where M is a predetermined natural number, the modifying step comprising the steps of:

modifying the multiple of A; and

subtracting the value MB from the multiple of C.

8. The method claimed in claim 5, wherein the C/B represents a repeating decimal.

9. A digital circuit for generating a multiple of a unit U, N times U, where U is a rational number and N is a natural number, comprising:

first, second and third registers for storing values A, B and C, respectively, where A, B and C are natural numbers, $A > 1$, $B > C$ and $U = A + C/B$;

first and second calculating circuits for generating a multiple of *A*, *N* times *A*, and a multiple of *C*, *N* times *C*, respectively;

a subtractor for generating a difference between the multiple of *C* and the value *B*; and

a modifying circuit for modifying the multiple of *A* according to the output of the subtractor,

wherein the first calculating circuit outputs the modified multiple of *A* as the multiple of *U*.

10. The digital circuit claimed in claim 9, wherein:

the first calculating circuit comprises an accumulator and an adder that adds the value stored in the first register to the value stored in the accumulator; and

the modifying circuit directs the adder to add +1 to its output when the output of the subtractor represents that the multiple of *C* is equal to or larger than the value *B*.

11. The digital circuit claimed in claim 9, wherein:

the first calculating circuit comprises an accumulator and an adder;

the modifying circuit comprises an adjusting circuit for adjusting the value stored in the first register with reference to a predetermined value, and a selector for selecting one of the outputs of the adder and the adjusting circuit according to the output of the subtractor; and

the adder adds the value stored in the accumulator to the output of the selector.

12. The digital circuit claimed in claim 9, wherein:

the first calculating circuit comprises an accumulator and an adder;

the modifying circuit comprises a fourth register for storing a value which is different from the value *A*, and a selector for

selecting one of the values stored in the first and fourth registers according to the output of the subtractor; and

the adder adds the value stored in the accumulator to the output of the selector.

13. The digital circuit claimed in claim 9, wherein the C/B represents a repeating decimal.

14. A digital circuit for generating a dependent variable of a periodic function whose independent variable is a multiple of a unit U, N times U, where U is a rational number and N is a natural number, comprising:

first, second and third registers for storing values A, B and C respectively, where A, B and C are natural numbers, $A > 1$, $B > C$ and $U = A + C/B$;

first and second calculating circuits for generating a multiple of A, N times A, and a multiple of C, N times C, respectively;

a subtractor for generating a difference between the multiple of C and the value B;

a modifying circuit for modifying the multiple of A according to the output of the subtractor; and

a memory device for storing a function table which represents relationship between the dependent and independent variables of the periodic function and for outputting a value corresponding to the modified multiple of A on the function table as the dependent variable corresponding to the multiple of U.

15. The digital circuit claimed in claim 14, wherein:

the first calculating circuit comprises an accumulator and an adder that adds the value stored in the first register to the value stored in the accumulator; and

the modifying circuit directs the adder to add +1 to its output when the output of the subtractor represents that the

multiple of C is equal to or larger than the value B.

16. The digital circuit claimed in claim 14, wherein:

the first calculating circuit comprises an accumulator and an adder;

the modifying circuit comprises an adjusting circuit for adjusting the value stored in the first register with reference to a predetermined value, and a selector for selecting one of the outputs of the adder and the adjusting circuit according to the output of the subtractor; and

the adder adds the value stored in the accumulator to the output of the selector.

17. The digital circuit claimed in claim 14, wherein:

the first calculating circuit comprises an accumulator and an adder;

the modifying circuit comprises a fourth register for storing a value which is different from the value A, and a selector for selecting one of the values stored in the first and fourth registers according to the output of the subtractor; and

the adder adds the value stored in the accumulator to the output of the selector.

18. The digital circuit claimed in claim 14, wherein the C/B represents a repeating decimal.